IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.: 10/065,723 Applicant(s): Batson et al.

Filed.: November 13, 2002 Art Unit: 2133

Dkt. No.: FIS920010179 Examiner: Stephen M. Baker

Title: **MEMORY DEVICE WITH DATA LINE STEERING AND BITLINE REDUNDANCY**

Honorable Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. 1.131

We, the applicants in the above-identified patent application, declare as follows:

1. That we are the applicants of the above-identified patent application, and inventor of the subject matter described and claimed therein.

2. That we conceived on Date X and actually reduced to practice on Date Y, a content addressable memory including: a set of bitlines; a set of data lines; a coupling circuit that directly connects each respective data line to a first respective bitline or to a second respective bitline based on a steering signal, the second respective bitline being adjacent to the first respective bitline; and a circuit that maintains the first respective bitline at a desired potential after the data line is coupled to said second bitline and as more particularly claimed in the above-identified patent application.

3. Both Date X and Date Y were prior to the filing date of May 10, 2002 of U.S. patent No. 6,714,429 to Srinivasan.

4. That, the actual reduction to practice of Date Y is evidenced by Exhibit A, an IBM

IBM invention disclosure describing the invention and including circuit diagrams generated using a software based circuit design system normally used to design IBM products.

5. That each date redacted from Exhibit A is prior to May 10, 2002.

6. That from about Date Y through November 13, 2003, the filing date of this application, we engaged in a diligent and reasonably continuous effort of extensive engineering including preparation of numerous drawings and simulations of the circuit in accordance with the invention.

7. Declarant's further state that the above statements were made with the knowledge that willful false statements and the like are punishable by fine and/or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statement may jeopardize the validity of this application or any patent resulting therefrom.

Date: 12-02-2005 Kevin A. Batson

Kevin A. Batson

Date: 12-01-2005 Robert E. Busch

Robert E. Busch

Date: 12-01-2005 Gary S. Koch

Gary S. Koch

Date: 12-01-2005 Fred J. Towler

Fred J. Towler

Date: 12/01/2005. Reid A. Wistort

Reid A. Wistort

Exhibit A

Main Idea for Disclosure BUR8-2000-0588
Prepared for and/or by an IBM Attorney - IBM Confidential
Archived On: [redacted]
DATE Y

Title of disclosure (in English)
(PF/CAM#7/MB) Bit line redundancy by steering bit and search lines

Idea of disclosure
1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.
THIS DISCLOSURE WAS RATED SEARCH AT THE CAM SCRUB SESSION HELD IN BURLINGTON ON [redacted]

DATE X

IBM CONFIDENTIAL
INVENTION DISCLOSURE

Inventors: Fred Towler, Kevin Batson, Rob Busch, Gary Koch, Reid Wistort

Title: (PF/CAM#7/MB) Bit line redundancy by steering bit and search lines

[redacted]

Problem Solved:

The invention described herein teaches a means for CAM column redundancy.

Background of Invention:

Until recent years, CAM arrays have been relatively small and therefore redundancy schemes have not been needed.

US patent 5796662 discloses a means for bit replacement in RAMs. A local latch is added for each datablt which stores a 1 or 0 state, indicating whether that datablt is good (functional) or bad (needs replacement). Circuitry is added which is responsive to this

[redacted]

information that will either allow the bit to operate normally or be replaced by the following means: sense amplifiers are connected to steering muxes that are connected to both a data bit 'A' as well as a databit 'A+1' (its adjacent neighbor). If databit 'A' is good, the sense amplifier is connected directly to databit 'A'. If databit 'A' is bad, the redundancy latch will be set to control the steering muxes so that the sense amplifier is connected to databit 'A+1'. Once this replacement is established, all steering muxes and corresponding redundancy latches are set so that databit 'A+2' thru 'A+n' are shifted by one as well. A similar steering mux is used to steer the data in path datalines around bad bits.

For CAM arrays using a CAM cell having bit and search lines, the steering mechanism just described will cause search data to be steered as well. The subject matter of this invention teaches a method of assuring that the 'bad' search lines are held low when being replaced so that search operations are not affected by data on the 'bad' searchline.

Figure 1 illustrates an example embodiment of the previously described invention using 2 levels of data steering.

Description of Invention:

This invention resides within the data line steering boxes shown in figure 1 the bit and search lines are fed from a common dataline. Figure 2 illustrates the invention. A steering mechanism (shown as a switch) controls how the datalines are connected to corresponding databit. For instance, data in 0(D0) can be connected to either databit 0 or 1(DB0/DB1). The steering mechanism shown operates as described in the background section. The novelty resides in the ability to assure that bad search lines are held low when being replaced so that search operations are not affected by data in the bad cells.

To achieve this, some circuitry is added that evaluates how the steering switches are set. As previously described, when a databit is bad, the corresponding dataline is steered to the adjacent dataline. All subsequent lines are also shifted. By comparing adjacent databit latches, the bad databit can be isolated and tied to ground. This scenario is shown in figure 2. In this scenario, databit 2 is determined to be bad. This is indicated by loading a '1' onto Latch output L2 and all subsequent latches. By inverting latch output L1 and performing an AND with L2, the pull-down transistor is activated and pulls the bad dataline 2 to ground. D0 and D1 are connected to their respective datalines via the blue switch connection and D2 and D3 are connected to their respective datalines via the red, shifted switch connection.

[redacted]

This method avoids a bad floating search line. The technique as shown can be implemented with other logic and also applies to both true and complement data signals and the corresponding output signal. Also, several levels of switches may be used to implement more redundancy capability.

Figure 3 illustrates a circuit schematic that enables the invention. A power UP signal (PUP) is provided to precondition the steering latch. Scan In (SIN) and Scan In complement (SINN) signals are provided to setup the steering mechanism (other techniques may be used). The pull-down circuitry is implemented by a NOR gate whose output provides the pull-down signal to the steering switches (PULLDN). The NOR input is from the steering latch and the previous data bit's steering latch (SOUTP). The NOR circuit provides a comparison between adjacent data bits to determine if one of them has been set to identify a bad bit, and if so, steering is required. If both bits are good, the pull-down signal is inactive and data flows in through DIN (true) and GIN (complement) and flows onto databitD0 (true) and G0 (complement). If one of the bit lines is bad, the pull-down signal is active and data still flows in through DIN (true) and GIN (complement) and but flows onto dataline D1 (true) and G1 (complement) via the steering mechanism previously described. Also, transistors T12 and T13 are activated thereby pulling down the bad datalines which drive the search lines.

Key Elements of Invention:

A means for databit redundancy by using bit steering with the capability of pulling down search lines determined to be bad.

Figures:

[redacted]

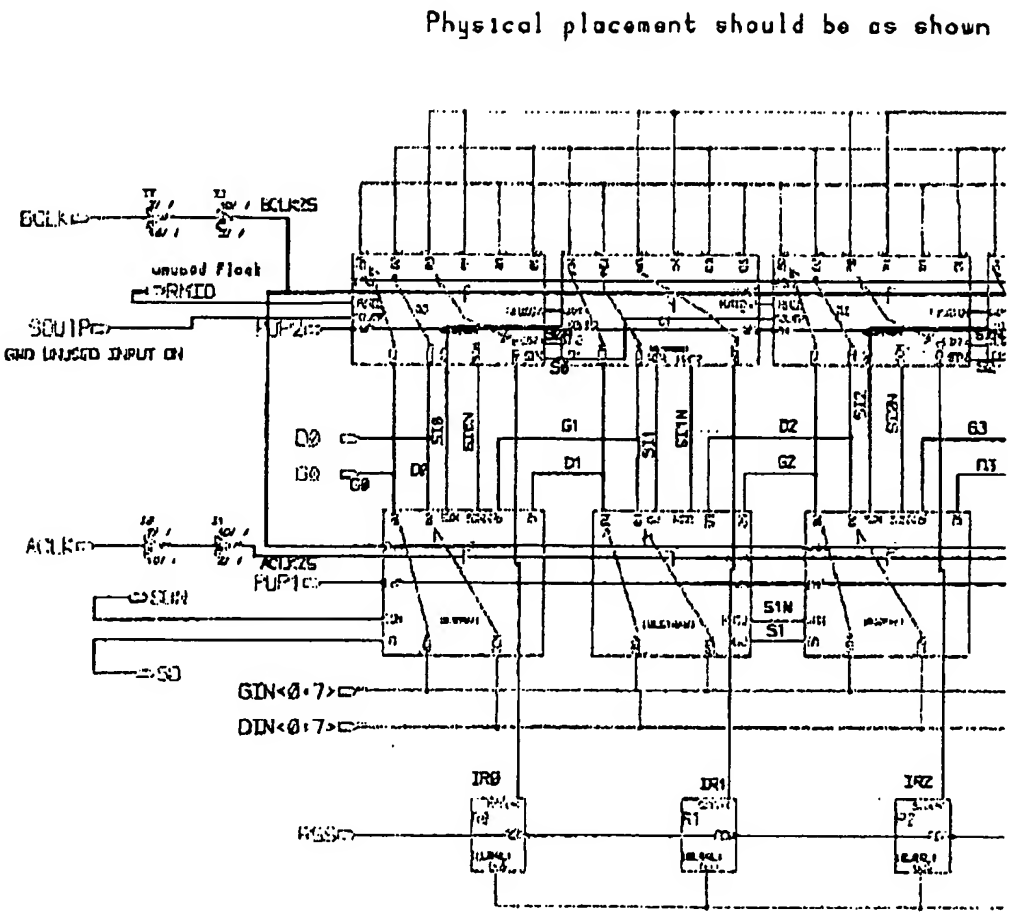

Figure 1.

[redacted]

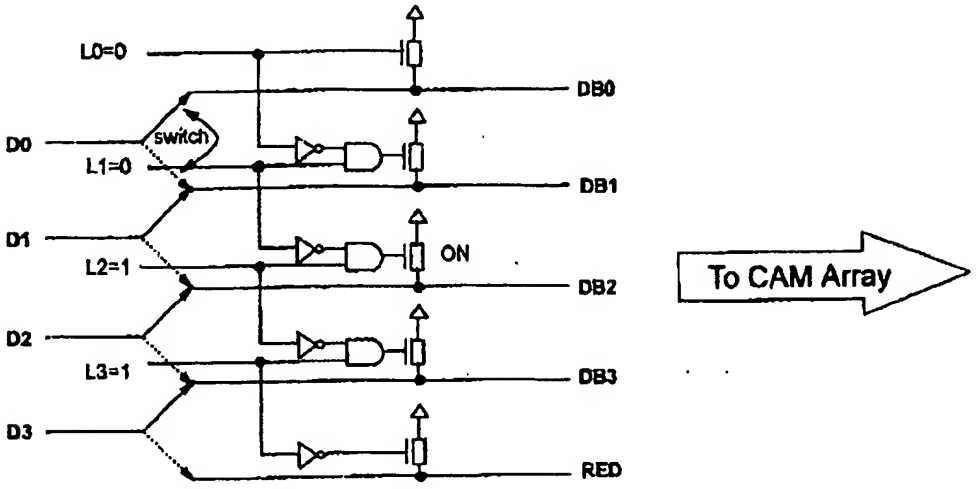

Figure 2.

[redacted]

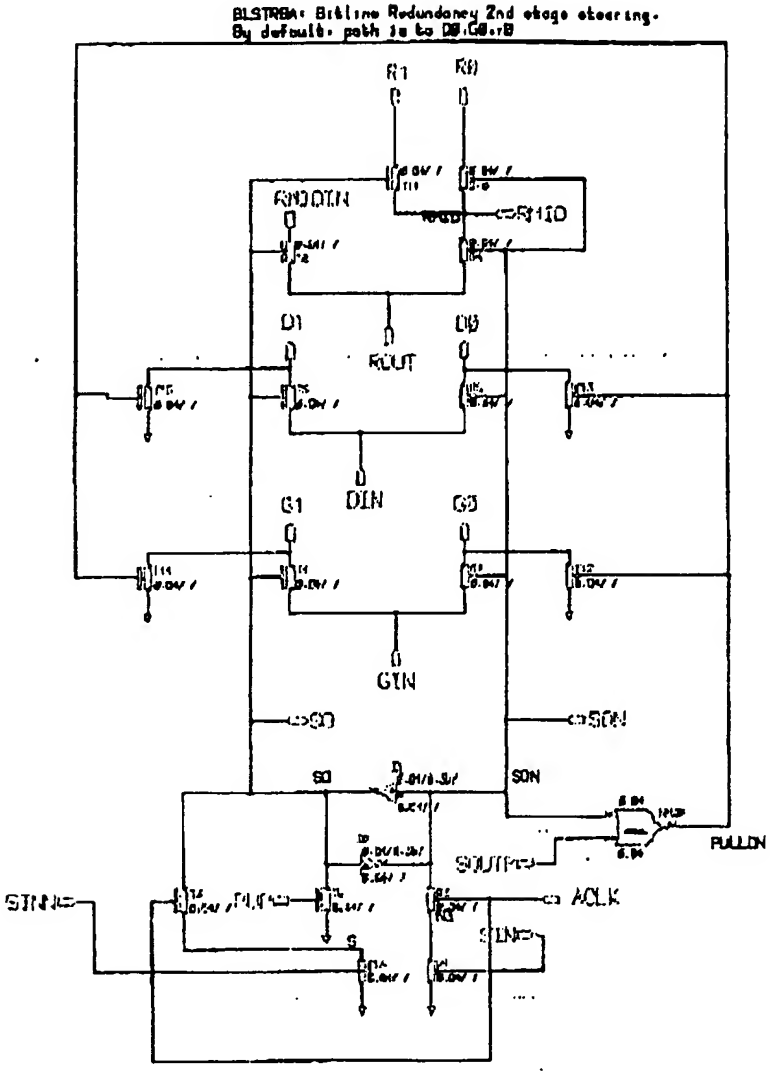

Figure 3.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

[redacted]